

FPA-320x256-CLCC InGaAs Array

Version V1.00

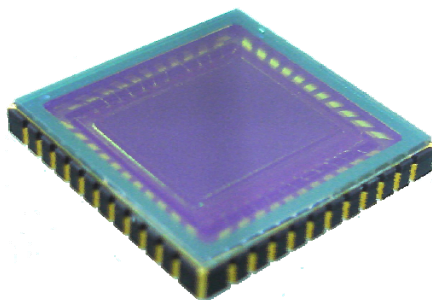
NEAR INFRARED (0.9um-1.7um) IMAGE SENSOR

FEATURES

- Room Temperature Operation
- 320x256 Array Format
- Light Weight 44CLCC Package
- Hermetic Sealed Glass Lid
- Typical Pixel Operability >99.5%
- Quantum Efficiency >70%

APPLICATIONS

- Near-infrared Imaging
- Imaging Spectroscopy
- Covert Surveillance
- Semiconductor Inspection
- Medical Science and Biology
- Fiberoptic Telecommunication
- Astronomy and Scientific
- Industrial Thermal Imaging
- Moisture Mapping



GENERAL DESCRIPTIONS

PARAMETER	VALUE
Sensor Technology	Standard InGaAs/InP
Spectral Range	0.9um-1.7um
Image Format	320(H)x256(V)
Pixel Size	30umx30um (>99% Fill Factor)
Image Size	9.6mm(H)x7.68mm(V)
Package Type	44-pin Ceramic LCC
Weight	1.6g

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FPA CHARACTERISTICS ($T_a=25^{\circ}\text{C}$)

PARAMETER	TYPICAL	CONDITIONS
Dark Current	< 0.4pA	0.1Volt detector bias
Quantum Efficiency	$\geq 70\%$	$\lambda=1.0\mu\text{m}-1.6\mu\text{m}$
Fill Factor	>99%	
Adjacent pixel crosstalk	<1%	
Detectivity	$\geq 5 \times 10^{11}$ Jones	$T_{\text{int}}=16\text{ms}$, High Gain, $\lambda=1.55\mu\text{m}$
Response Nonuniformity	$\leq 10\%$	Under 50% Saturation
Nonlinearity (Max. Deviation)	$\leq 2\%$	10%-90% Full Well Capacity
Max. Pixel Rate	10MHz	
Gain	High: 13.3 $\mu\text{V}/e^-$ Low: 0.7 $\mu\text{V}/e^-$	
Pixel Operability*	> 99.5%	Dark Current $\leq 20\%$ Full Well Response Nonuniformity $\leq 20\%$

* Pixel Operability is defined with edge pixel excluded.

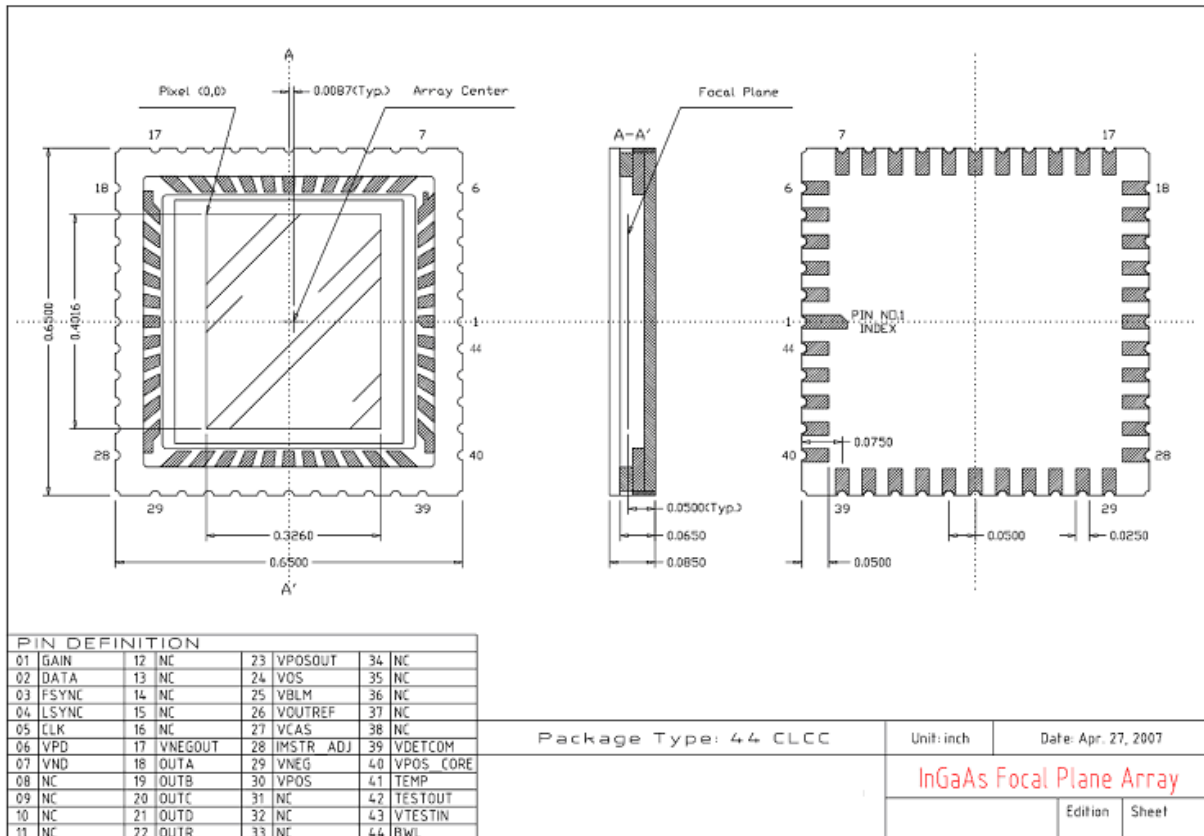
ABSOLUTE MAXIMUM RATINGS

PARAMETER	UNIT	MIN	MAX
Operation Temperature	$^{\circ}\text{C}$	-20	85
Storage Temperature	$^{\circ}\text{C}$	-40	85
Power Consumption	mW	---	175

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PACKAGE OUTLINE



Note : ID number of the imager is printed on the backside of the package.

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OPERATING CONDITIONS

Bias Input

Pin #	Bias	Voltage	Current	Remark
6	VPD	5.5V	<1mA	Logic positive supply
7	VND	0V	<1mA	Logic negative supply
23	VPOSOUT	5.5V	<25mA	Output stage analog supply
17	VNEGOUT	0V	<25mA	Output stage analog ground
30	VPOS	5.5V	<5mA	Positive analog supply
29	VNEG	0V	<15mA	Negative analog supply and substrate
40	VPOS_CORE	5.5V	<15mA	CTIA amplifier positive supply
39	VDETCOM	4.7V - 5.5V	<5mA	Detector common voltage Detector bias = VDETCOM-4.7*

*VDETCOM lower than 4.7V will forward bias the sensor

Digital Pattern Input

Pin #	Clocks	Levels	Rise/Fall	Remark
5	CLK	0V - 5.5V	<10ns	Master clock Max. Freq.=5MHz
3	FSYNC	0V - 5.5V	<10ns	Frame sync - controls frame start and integration time
4	LSYNC	0V - 5.5V	<10ns	Line sync - controls line readout timing
2	DATA	0V - 5.5V	<10ns	Data code input - programs device function registers in Control Mode Left open in Default Mode

Clocks	Synchronization
FSYNC	Rising and falling when CLK is rising
LSYNC	Rising and falling when CLK is falling
DATA	Rising (falling) when CLK is rising (falling)

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Video Output

Pin #	Outputs	Levels	Settle	Remark
18	OUTA	1.4V to 4.1V	<50ns to 0.1%	Output A used in single output mode
19	OUTB	1.4V to 4.1V	<50ns to 0.1%	Output A and B used in two output mode
20	OUTC	1.4V to 4.1V	<50ns to 0.1%	Output A, B, C, and D used in four output mode
21	OUTD	1.4V to 4.1V	<50ns to 0.1%	Output A, B, C, and D used in four output mode
22	OUTR	3V	-	Reference for common mode output

Gain & Bandwidth Selection in Default Mode

Pin #	Functions	Low	High	Remark
1	GAIN	0V C=10fF	5.5V C=210fF	Selects unit cell integration capacitor Left open in Control Mode
44	BWL	0V Low BW	5.5V High BW	Selects bandwidth limiting capacitor in unit cell Left open in Control Mode

Advanced Function

Pin #	Functions	Voltages	Remark
27	VCAS*	3.75V	CTIA amplifier cascode FET bias
26	VOUTREF*	3V	Output reference level during blanking period
25	VBLM*	2V	Detector bloom control
28	IMSTR_ADJ**	0V - 5.5V	Adjusts analog master bias current
24	VOS	0V - 5.5V	Variable Offset/Skimming Control Voltage
41	TEMP	0V - 5.5V	On chip temperature monitor 0.74V at 300K, Slope=-14.8mV/10K in 50-300K
43	VTESTIN	1.5V - 4.5V	For use in IC function test
42	TESTOUT	0V - 5.5V	Left open in FPA operation

*Internally generated after bias input, but can be overridden.

** Also addressable through control register (DATA).

[http:// www.jmsienna.com](http://www.jmsienna.com)
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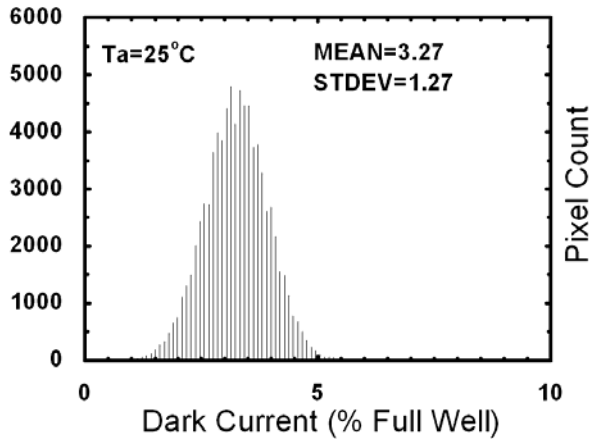
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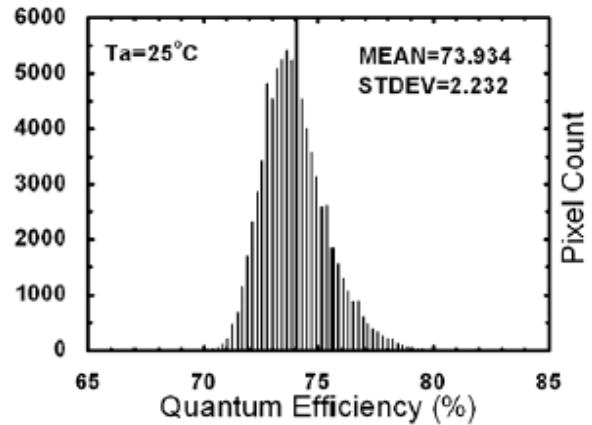
EXAMPLE CURVES

Statistical Histogram of Dark Current



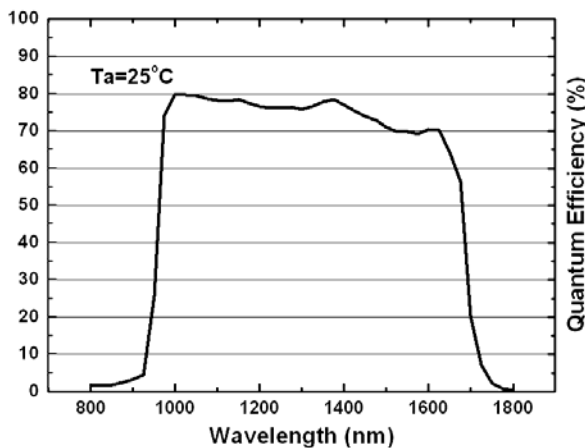
Test Conditions:	
Illumination	Dark
Wavelength	---
Gain	Low
Integration Time	16ms
Remark	Effective Screen

Statistical Histogram of Quantum Efficiency



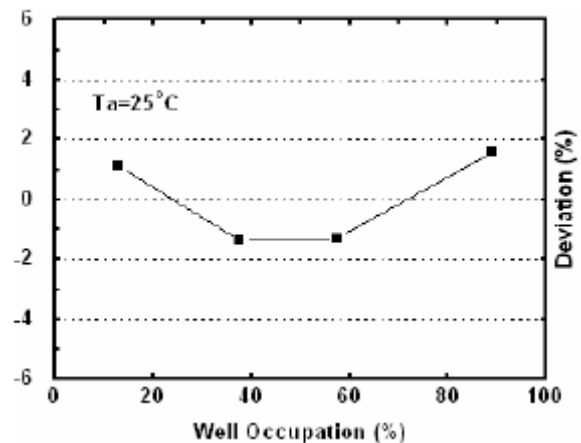
Test Conditions:	
Illumination	Nonuniformity $\leq\pm 0.15\%$
Wavelength	1310nm
Gain	Low
Integration Time	For 50% Saturation
Remark	Effective Screen

Quantum Efficiency Spectrum



Test Conditions:	
Illumination	Nonuniformity $\leq\pm 0.15\%$
Wavelength	Broadband
Gain	Low
Integration Time	2ms
Remark	Effective Screen Array Average

Linearity



Test Conditions:	
Illumination	Nonuniformity $\leq\pm 0.15\%$
Wavelength	1310nm
Gain	Low
Integration Time	---
Remark	Effective Screen Array Average

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TIMING CHART FOR DEFAULT MODE OPERATION

